

IN THE CLAIMS

1. (Currently amended) A processor device for processing instructions, in particular very long instruction word (VLIW) instructions, comprising:

memory means for storing instruction words, each instruction word consisting of segments,

fetching means for fetching instruction words from said memory means, and
executing means for executing instructions in accordance with instruction words fetched from said fetching means.

~~characterized in that~~ wherein said fetching means is adapted responsive to a previously-fetched header to fetch essentially those segments of an current instruction word (line i)-only which contain relevant information, without regard to a next instruction word.

2. (Previously presented) The device according to claim 1, wherein said memory means is adapted to store instructions words of a kind where the instruction words have the same code size density.

3. (Previously presented) The device according to claim 2, wherein said memory means is adapted to store non-compressed instructions words.

4. (Previously presented) The device according to claim 1, wherein said memory means comprises a plurality of memory portions wherein each memory portion is provided to store one segment of an instruction word, and said fetching means is adapted to access

those memory portions only which contain relevant information.

5. (Previously presented) The device according to claim 1, wherein said memory means includes a plurality of lines, each line being provided for storing a complete instruction word.

6. (Previously presented) The device according to claim 4, wherein the width of said memory means is divided over all lines into memory units in accordance with different segments of the instruction words so that each memory unit is formed by memory portions for storing instruction word segments of the same order and/or kind.

7. (Previously presented) The device according to claim 4, wherein all segments of the instruction words and said memory means have the same width, and each memory portion forms a separate line for storing an instruction segment.

8. (Previously presented) The device according to claim 4, wherein each line of said memory means is divided into said memory portions in accordance with different segments of the instruction words so that each memory portion is provided for storing one segment of an instruction word.

9. (Currently amended) A method for processing instructions, in particular very long instruction word (VLIW) instructions, in a processor device, comprising the steps of

storing instruction words in a memory means, each instruction word consisting of segments,

fetching instruction words from said memory means, and

executing instructions in accordance with instruction words fetched from said fetching means,

wherein said fetching means is responsive to a previously-fetched header to fetch essentially those segments of a current instruction word only which contain relevant information, without regard to a next instruction word~~characterized in that essentially those segments of an instruction word are fetched only which contain relevant information.~~

10. (Previously presented) The method according to claim 9, wherein the instruction words have the same code size density.

11. (Previously presented) The method according to claim 10, wherein the instructions words are not compressed.

12. (Previously presented) The method according to claim 9, further comprising the step of dividing said memory means into a plurality of memory portions wherein each memory stores one segment of an instruction word.

13. (Previously presented) The method according to claim 9, further comprising the step of dividing said memory means into a plurality of lines, wherein each line stores a

complete instruction word.

14. (Previously presented) The method according to claim 12, further comprising the steps of dividing the width of said memory means over all lines into memory units in accordance with different segments of the instruction words, and forming each memory unit by memory portions for storing instruction word segments of the same order and/or kind.

15. (Previously presented) The method according to claim 12, further comprising the steps of providing all segments of the instruction words and said memory means with the same width, and adapting each memory portion so as to form a separate line for storing an instruction segment.

16. (Previously presented) The method according to claim 12, further comprising the steps of dividing each line of said memory means into said memory portions in accordance with different segments of the instruction words, and adapting each memory portion so as to store one segment of an instruction word.